LISTING OF THE CLAIMS:

(Claims 1-36 have been cancelled)

37.(Previously Presented) A method of improving data retention in a nonvolatile writeable memory having an erased-cell reference level and a programmed-cell reference level, the nonvolatile writeable memory having a plurality of memory cells, each of the memory cells being in an erased state when storing a charge below the erased-cell reference level, and each of the memory cells being in a programmed state when storing a charge above the programmed-cell reference level, the method comprising the steps of:

(a) identifying a memory cell having a charge above the erased-cell reference level and below the programmed-cell reference level; and

(b) programming the memory cell until the charge of the memory cell is above the programmed-cell reference level.

(Claim 38 has been cancelled)

39.(Previously Presented) A method of improving data retention within a non-volatile writeable memory, the method comprising the steps of:

(a) identifying a group of one or more memory cells having a stored charge over a first threshold and less than a second threshold; and

(b) programming each memory cell of the group of one or more cells until each of the memory cells has a stored charge over the second threshold.

40.(Previously Presented) The method of claim 39 wherein the first threshold corresponds to an erased-cell reference level plus a guardband level.

41.(Previously Presented) The method of claim 37 wherein the identifying corresponds to identifying a memory cell having a charge above the erased-cell reference level plus a guardband level.

42.(Previously Presented) A method of improving data retention in a nonvolatile writable memory having a first reference level and a second reference level, the

nonvolatile writable memory having a plurality of memory cells, each of the memory cells being in an first state when storing a charge below the first reference level, and each of the memory cells being in a second state when storing a charge above the second reference level, the method comprising:

writing into each of a set of the plurality of memory cells a respective data value, wherein the data values are one of the first and second states;

identifying a memory cell of the set having a charge above the first reference level and below the second reference level; and

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rewriting the respective data value into the memory cell.

43.(Previously Presented) The memory of claim 42, further having a third reference level intermediate between the first and second reference levels, wherein the identifying comprises identifying a memory cell of the set having a charge above the third reference level and below the second reference level.

44.(Previously Presented) The memory of claim 43, further having a fourth reference level intermediate between the second and third reference levels, wherein the identifying comprises identifying a memory cell of the set having a charge above the third reference level and below the fourth reference level.

45.(Previously Presented) The memory of claim 42, wherein the rewriting comprises determining the respective data value to rewrite into the data cell using error correction code.

46.(Previously Presented) A method of improving data retention in a nonvolatile writable memory having a first reference level and a second reference level, the nonvolatile writable memory having a plurality of memory cells organized into sectors, each of the memory cells being in an first state when storing a charge below the first reference level, and each of the memory cells being in a second state when storing a charge above the second reference level, the method comprising:

accessing a first sector of said memory cells;

identifying a second sector of said memory cells having one or more memory cells with a charge above the first reference level and below the second reference level; and

rewriting the data values stored in the memory cells of the second sector.

47.(Previously Presented) The memory of claim 46, wherein said accessing a first sector of said memory cells comprises programming data values into said memory cells of the first sector, wherein the data values are one of the first and second states

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48.(Previously Presented) The memory of claim 46, wherein said accessing a first sector of said memory cells comprises reading the data values stored in said memory cells of the first sector, wherein the data values are one of the first and second states

49.(Previously Presented) The memory of claim 46, wherein said second sector is chosen at random prior to said identifying.

50.(Previously Presented) The memory of claim 46, wherein a memory cells of said first sector shares a common bit line with a memory cell of said second sector.